



COPY OF PAPERS
ORIGINALLY FILED

T.D. 0500
#3
Cebenko 1-1-3-1-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): S.R. Cebenko et al.
Case: 1-1-3-1-1
Serial No.: 10/082,050
Filing Date: February 14, 2002
Group: 2836
Examiner: To Be Assigned

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature: Senise A. Gleaser Date: May 7, 2002

Title: Integrated Circuit Base Transistor Structure
and Associated Programmable Cell Library

TRANSMITTAL OF FORMAL DRAWINGS

Assistant Commissioner for Patents
Washington, D.C. 20231

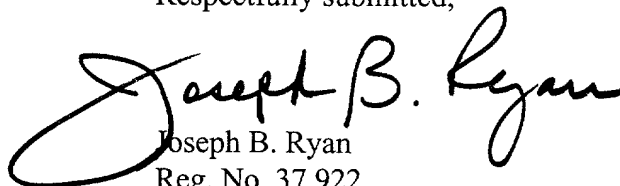
Attention: Official Draftsperson

Sir:

In response to the Notice to File Corrected Application Papers dated March 19, 2002, Applicants submit herewith four (4) sheets of formal drawings to complete the above-referenced patent application.

A copy of the Notice is enclosed herewith. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Ryan, Mason & Lewis, LLP** Deposit Account No. **50-0762** as required to correct the error.

Respectfully submitted,



Date: May 7, 2002

Joseph B. Ryan
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
Attorney for Applicant(s)
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517